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Enhancing Observability of Signal Composition and Error Signatures during Dynamic SEE Analog to Digital Device Testing

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***Abstract*—A novel approach to dynamic SEE ADC testing is presented. The benefits of this test scheme versus prior implemented techniques include the ability to observe ADC SEE errors that are in the form of phase shifts, single bit upsets, bursts of disrupted signal composition, and device clock loss.**

***Index Terms*— SEE, ADC, FPGA, Dynamic**

I. Introduction

ANALOG to digital converters (ADCs) are widely utilized in critical space applications. As a part of the device selection process, it is essential to perform error-rate calculations to determine if the device will satisfy system requirements while operating in harsh radiation environments. Error rate calculations for such environments are based on the device's Single Event Effects (SEE) characterization and associated SEE cross-sections. SEE cross-sections are generally calculated by counting error events as the devices under test (DUTs) are irradiated. Parameters used in SEE rate calculations are the number of error events per particle fluence, linear energy transfer (LET) of particles, and the targeted environment. A caveat to this approach is that it can over-simplify a complex characterization by not differentiating between error events. In order for flight-project designers to implement efficient mitigation strategies for ADC devices, it is equally important to categorize error signatures such as output signal amplitude response, signal phase-offset effects, and error duration as they vary among ADC technologies. Consequently, the granularity and accuracy of fault observation during SEE testing must be robust.

Over the years, various approaches have been used to test ADC SEE sensitivity [1]-[4]. The plethora of approaches is a direct result of the absence of a standardized test methodology that stipulates test conditions such as: input signal activity (dynamic versus static), clock sample rates, error signature characterization, and test vehicle noise filtration. The lack of a standard test methodology can result in Single Event Upset (SEU) cross-section calculations that significantly deviate from one another and mischaracterize the device's complete radiation response. As a result, inaccurate device error prediction rates can be generated, substandard devices for critical applications can be utilized, and missions can consequently be compromised.

In response to the growing need of ADC SEE test enhancement and standardization, the NASA Goddard Radiation Effects and Analysis Group (REAG) has investigated and developed a variety of ADC SEE test schemes. This paper is a synopsis of one of the REAG testing strategies referred to as the Four Point Windowing Scheme (FP). The FP SEE test methodology is novel and has demonstrated advantages over other ADC SEE test schemes. Benefits of FP include its enhanced ADC output observability and error event differentiation during SEE testing.

All FP SEE tests were implemented using the NASA Goddard Radiation Effects and Analysis Group's (REAG) Low Cost Digital Tester (LCDT) as a test vehicle. The FP testing technique has been applied to ADC devices from two separate manufacturers: Texas Instruments ADS5424 14-bit ADC [5] and National Semiconductors' ADC14155 14-bit ADC [6]. It should be noted that both devices can sample signals with rates greater than 100MHz. Slower ADC devices would generally be used to sample near static signals. The strength of high speed ADCs such as the ADC14155 and the ADS5424 is to sample and process complex signals that contain a broad frequency spectrum. Subsequently, this manuscript will focus on sampled ADC output signal composition of high-speed signals subject to radiation and

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potential SEE.

The content of this paper provides a brief section regarding ADC background and critical system implementation requirements. A section dedicated to test process development and test-bed implementation follows. The paper concludes with radiation test results, analysis, and future development of the FP methodology.

II. BACKGROUND

A. General ADC Operation within Systems

The purpose of using an ADC within a system is to convert an analog signal, into a sampled digital signal, x(n), in order to perform robust processing in the digital domain. To facilitate computations, signal processing is generally applied to x(n) in the frequency domain (X(k)). Computer systems generally use Discrete Fourier Transforms (DFT) (or some form thereof such as Fast Fourier Transforms (FFT)), to manipulate the phase and amplitude spectra of sampled signals. The DFT of a sampled input signal, x(n), is performed on a discrete number of samples (N). If the sampling frequency is fs and there are N samples taken, then the frequency spectrum X(k) generated by the DFT will consist only of values at kfs/N where k=0… N-1 [13],[14]. Therefore, if there are N time-samples of x(n) then there will also be N X(k) frequency transformations. It is important to note that the conversion will be inaccurate if any points are missing. Therefore (1) must be satisfied.

$$\exists x(n) \forall \quad n = 0 \ldots N-1 \qquad \exists X(k) \forall \; k = 0 \ldots N-1 \tag{1}$$

The DFT is defined in (2) [13][14].

$$X(k) = \sum_{n=0}^{N} x(n) \cdot e^{-j2\pi nK/N} \tag{2}$$

Pertaining to (2), each X(k) element will have an amplitude component and a phase component. SEUs generated in the ADC's sample clock circuitry can dissatisfy (1) by loss of sample outputs or impact sample timing resulting in erroneous phase offsets. Other types of SEUs can impact the digitized amplitude. It will be shown that amplitude effects can be so severe such that a signal can flatten for a significant number of ADC clock cycles. In either case, the designer must be aware of the event duration, event frequency, and type of possible errors due to SEUs.

In addition, because the complexity of DFT processing significantly increases as N increases, a design tradeoff must be made on the size of N. However, in the presence of SEUs, if N is too small (not enough samples per DFT processing cycle), then the affected X(k) elements may contain too much error. The consequence of not obtaining enough samples can potentially amplify the upset in the frequency domain (or reduce averaging capability) and might subsequently cause catastrophic events. One example of such an event is a filter processing the inaccurate X(k) information causing a feedback system to become unstable.

Based on system implementation, and possible error signatures, more complex implementation schemes may be necessary. In order to employ the proper functionality, ADC SEU noise must be well characterized for amplitude, phase, and output continuity. The following sections describe possible ADC noise regarding normal operation and the additional impact of SEE.

B. The Characteristics of ADC Parametric Noise versus SEE Noise

Typical manufacturer ADC parametric characterization involves measuring error generated by quantization noise together with other noise sources such as jitter, non-linearities, fixed pattern noise, reference voltage irregularities, power supply variations, missing codes, and thermal noise [8]-[12]. There are several measurements that characterize how the noise levels affect both the phase and amplitude of the ADC output under various operational conditions[8]-[11]. Two very common error measurements performed by the manufacturer are the Signal to Noise Ratio (SNR) and the Effective Number of Bits (ENOB). Parametric noise is minimized by the manufacturer however it is always present under normal ADC operation. It is considered to be spread throughout every cycle of the ADC output and if enough cycles of the ADC output are analyzed, the characterization is reliable and most importantly, repeatable. The designer compensates for ADC SNR and ENOB by filtration, mitigation, or allowance of specified system error.

During device irradiation, parametric degradation can occur after the device has endured a certain amount of dose. The amount of dosage required to reach degradation is specific per device and can be measured via Total Ionizing Dose (TID) testing. It will be illustrated that during SEE testing and prior to parametric-degradation, the tested ADC devices were able to recover to normal operation after experiencing SEEs. It will also be demonstrated that the major differences between SEEs and parametric noise are that ionizing particle strikes can perturb the output for multiple cycles with significantly greater values than normal parametric noise. However, the SEE perturbations only last for a discrete amount of time. In addition, the SEEs occur randomly and are not necessarily exactly repeatable. Consequently, because parametric testing evaluates a different set of conditions and device response than that of SEE analysis, implementing parametric tests for SEE evaluation will not produce comprehensive SEE information. Instead, an evaluation of signal decomposition, phase error, and their duration is essential.

In general, ADC SEEs can occur due to a transient in the ADC's analog or digital circuitry. Analog error signatures such as voltage regulation becoming instable or PLL strikes increasing output jitter will manifest at the ADC outputs and are distinct from digital SEEs. Other upsets such as digital clock transients causing many DFFs to lose their state will produce a temporary Single Event Functional Interrupt (SEFI). Therefore, SEE testing should be able to:

-- Check for code errors due to transient capture, DFF upset, or voltage reference upsets.

-- Detect jitter from PLL or other analog sampling clock upsets.

-- Detect clock upsets that can cause SEFIs

-- Detect complete disruption of ADC output or activity

As previously stated, because the SEEs are random, time-discrete upsets and are not spread throughout every cycle of ADC output (as with parametric noise), there must be enough information for each data cycle to capture and evaluate the nature of the various SEEs. It should also be noted that output transients can occur in the digital ADC output buffer; however, such errors have an insignificant cross-section as compared to other upsets and are categorized with code upsets for this study.

The purpose of this study is to monitor the severity of various SEU error signatures. It is expected that this SEE analysis be used in conjunction with the manufacturer's parametric evaluation as an additional noise source regarding filtration, mitigation, and general critical-system design considerations.

C. Design under Test (DUT) Architectures

As previously stated, the two DUTs that were evaluated were the ADC14155 [6] and the ADS5424 [5]. Both DUTs contain common elements such as PLL clocking circuitry and voltage references. However, data digitizing and correction circuitry are distinct. As an example of differentiation, the ADC14155 is a pipelined digitizer while the ADS5424 uses successive approximation.

III. SEE Test Methodology Evaluation

Regardless of the test methodology employed during SEE evaluation, it is important to filter the non-SEU noise generated from the test vehicle and the ADC device. Consequently, if each test consists of comparing the ADC output code (x_n) to an expected value, then compensation must be made due to inherent system error during the comparison process.

As a solution, prior to testing, system noise was measured for each test type. A minimal error-bound (EB) windowing each expected value was calculated per test set-up such that no ADC output code errors exist during operation and pre-irradiation. The EB code value can be translated to its corresponding voltage level (VEB) as illustrated in (3).

$$V_{EB} = \frac{EB * Vpp}{2^{Nb}} \quad (3)$$

Regarding (3), Nb is the number of ADC output bits and V_{PP} is the peak-to-peak manufacturer supplied voltage range.

Potential SEEs that fall within the EB window will not be observable. Therefore, to obtain maximum observability, it is essential to minimize test vehicle noise. EB values will change based on the test set-up, Number of ADC output bits, and the ADC DUT. SEE tests are performed with the minimum calculated EB, however, post processing of radiation data entails calculating SEU cross-sections at various EB values so that:

1. SEU ADC cross-sections obtained from different test vehicles with different noise characteristics can be compared by analyzing cross-sections with common VEB values.

2. SEU ADC cross-sections obtained from different ADCs with a different number of output bits can be compared by analyzing cross-sections with common VEB values.

3. The amplitude of ADC SEU code errors can be better analyzed. As an example, histograms can be developed binning amplitude errors within particular ranges.

The following sections will discuss three test methodologies that were investigated. As previously stated, all SEE tests utilized minimal EBs during radiation tests.

A. Single Point (SP) Test Scheme

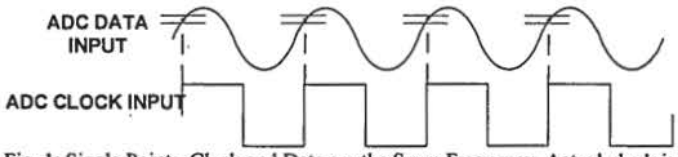

Fig. 1: Single Point - Clock and Data are the Same Frequency. Actual clock is the same sinusoid as the data input but is illustrated as a square wave for simplification of demonstrating sampling points.

The REAG approach to SP ADC SEE testing is to apply input excitation to the ADC clock and data connections from the same source (i.e. clock and data input signals are tied together). Clock frequency, fs, is strictly equal to data frequency, fd. Consequently, the ADC will theoretically always sample the same point as illustrated in Fig. 1. As a result, the data output of the ADC should stay near constant.

This test becomes advantageous because data and clock are generated from the same source; SP is simple to set up and has minimal test vehicle noise. For a 14-bit ADC, a minimal EB of 16 (1.95mv) was calculated for the implemented test vehicle. Let E be the expected value and x_n the ADC output code, then (4) is the SP comparison performed for every x_n in the LCDT.

$$\left(E - EB/2\right) < x_n < \left(E + EB/2\right) \quad (4)$$

B. Differential Points (DP) Test Scheme

The REAG approach to ADC SEE DP testing (otherwise known as Beat Frequency) [4][12] is to apply input excitation to the ADC clock and data connections from separate signal generators. The clock frequency (fs) is expected to gradually lag the data frequency (fd) such that the ADC output will slowly change. Hence, the difference between two consecutive ADC outputs (x_n and x_{n-1}) is expected to be minimal as illustrated in Fig. 2. It is important to note that the temporal difference between x_n and x_{n-1} is one ADC clock cycle. Additionally, one ADC clock cycle is slightly shorter than one data input sinusoid cycle.

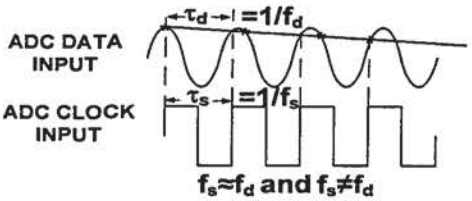

Fig. 2: DP (Beat Frequency [4]) Clock and Data Waveforms. Actual clock is a sinusoid but is illustrated as a square wave for simplification of demonstrating sampling points.

Equation (4) illustrates the DP relationship between the input signal frequency and the sample frequency for a 14 bit ADC.

$$fs = \frac{fd}{1 - \frac{1}{2^{Nb}\pi}} = 1.000019\,fd \qquad (5)$$

A minimal EB of 96 (11.7mv) was calculated for the implemented test vehicle. Equation (6) is the DP comparison performed for every x_n and x_{n-1} in the LCDT.

$$-\left(EB/2\right) < x_n - x_{n-1} < \left(EB/2\right) \qquad (6)$$

C. The Pros and Cons of SP and DP testing

The benefit of the SP and DP schemes is that they are relatively easy to implement. Both methodologies prove to be sufficient at counting errors during irradiation. As a result, general SEE error cross-sections are valid using these techniques and are currently used in critical missions for upper bound ADC error prediction. It is important to note that the error rates calculated via the SP and DP schemes represent all errors that fall outside of the error bound windows without differentiation between error signatures.

One concern about the SP method is that the same sample point within a data period is always sampled; whereas after thousands of cycles, the DP method can sample every point along a sinusoid input. However, it is important to note that the DP scheme only samples approximately one point per input data period (see (5)). Although a proven method for parametric testing, the DP method proves to provide similar cross-sections as the SP method at compatible Veb masks. Fig. 3 illustrates that the DP scheme and the SP scheme for a 14 bit ADC are statistically equivalent for similar EBs. In this figure, the DP cross-section with its minimal EB of 96 (11.7mv) has been compared to the SP cross-section with an EB of 128 (15.6mv). Two points contribute to the explanation of SP and DP similar cross-sections: (1) The resultant SEEs are faults that last for a discrete amount of time and are not consistent noise spread amongst all ADC data periods (as is ADC parametric noise); hence there is no advantage to DP testing (2) Both methods analyze approximately the same amount of input-data information per data cycle.

A problem with the DP method is that the test vehicle inherently has a greater amount of noise. This is a consequence of the necessity to synchronize two separate signal generators requiring fine granularity of frequency settings. The SP minimal EB is equal to 16 and the DP minimal EB is equal to 96. The relatively noisy DP test vehicle requires a larger EB and thus does not have the resolution of SEU observability as the SP. Filters can be used at the test vehicle level to reduce the noise [12]. However, implementation can be expensive, very complex, and may not provide much return because of the nature of SEEs and the amount of required data sampling per data input cycle.

As previously stated, the SP and DP methods provide overall error rates that are nonspecific per error type. Due to the complexity of ADC devices, a variety of error signatures can occur depending on the circuitry affected by the particle strike. Consequently, it is desirable to know how often particular errors can occur. Because only one point per data period is sampled in the SP and DP schemes, errors such as jitter, flattening, or small perturbations to the output signal composition are difficult to identify and differentiate.

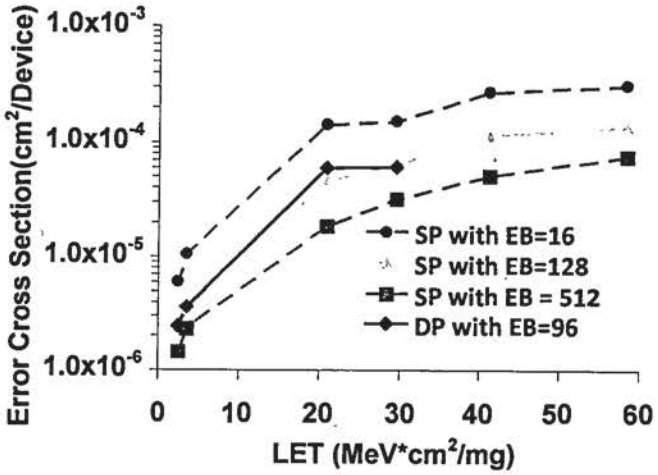

Fig. 3: SP and DP Cross-sections with various error mask (EB) values. The DP cross-section with EB = 96 is similar to the SP cross-section with EB=128. This illustrates that there is not much advantage to implementing DP when performing SEU testing.

D. Four Point (FP) Test Scheme

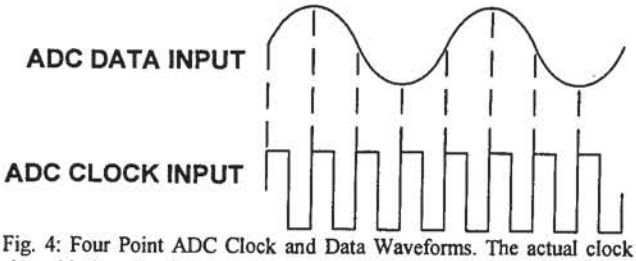

Fig. 4: Four Point ADC Clock and Data Waveforms. The actual clock is a sinusoid but is illustrated as a square wave for simplification of demonstrating sampling points.

As previously stated, evaluation of signal composition such as temporary signal flattening or temporary phase shifts requires more samples per data input period (fs>>fd). As a simplified first approach, REAG developed the FP test scheme. The algorithm of the FP scheme dictates that the relationship of input clock (fs) to input data (fd) is fs = 4·fd and is illustrated in Fig. 4. Consequently, four points are sampled per signal period.

As a direct result of over-sampling, the two dimensional nature of SEU errors (phase and amplitude) can be precisely tracked and critical design considerations can be examined such as: (1) Will the signal retain its composure (noisy output)? (2) Is the phase of the output signal affected? (3) Can there be complete loss of data output signal (flattening)? (4) Will the signal filtration system require a more complex design implementation? Because the focus of this paper is signal composition and observability during SEE testing, the rest of this manuscript will pertain to the test fixture and irradiation utilizing the FP methodology.

IV. FP Test System Implementation

This section concentrates on how the ADC FP test system was constructed. Attention to DUT architecture, test system noise, data capture, and data processing is discussed.

A. NASA REAG LCDT Test Vehicle

The LCDT has a Xilinx Spartan-3 FPGA core that can be configured to perform data processing with a variety of DUTs. Fig. 5 illustrates the simple interface between the LCDT and the ADC DUT. Connections that are monitored by the LCDT coming from the DUT are the Data bus (D(13:0))and the Data Ready (DRY) signals as illustrated in Fig. 5. The Data bus is a 14-bit 2's compliment digital representation of the analog signal. ADC DRY (1-bit digital signal) will appear at the output (after a specified latency) for every applied input clock cycle. The DRY is a copy of the input clock when output data is available. Input signals to the ADC DUTs are driven by two separate signal generators. The clock signal generator is the master source supplying the highest frequency and is considered the synchronizer. The Data signal generator is the slave and is forced to be synchronized to the master source via a cable connection between the two boxes. Both Clock and Data inputs are analog sine-wave signals and are continuous during irradiation.

As with the SP and DP test schemes, FP test and evaluation is an analysis of fluctuations, perturbations, or loss of the ADC output during irradiation. In order to detect ADC SEE digital outputs, a comparison to a digital reference is necessary. With a carefully contrived test system, it is possible to use the ADC output prior to irradiation as reference points. The synchronization of the clock and data signal generators, as previously described, is essential to analyze deviations of ADC output codes from its digital reference points. With proper synchronization and under normal FP device operation, the output of the ADC will have 4 distinct output codes that will contain small, yet bounded, deviations from their 4 expected values as illustrated in Fig. 4. Without proper synchronization, output codes will naturally drift with significant deviations in value and will thereby invalidate the utilization of reference points for comparison purposes. Subsequently, 4 expected (reference) values are calculated by averaging millions of cycles of the ADC sampled outputs prior to every radiation test. A detailed description of the FP expected value calculations is provided in Section IV.B.

The FP algorithm implemented within the FPGA tester core has two phases: (1) A preprocessing phase that includes expected value calculations and (2) An irradiation phase that includes filtration and data processing. The FP technique requires constructing windows that are temporally 4 ADC clock cycles long in order to simultaneously evaluate 4 consecutive ADC output samples. The samples are expected to track the input analog sine-wave. The tester is able to evaluate every clock cycle of data and report every cycle of error. This facilitates burst analysis with the granularity of a clock cycle.

The following section provides a more detailed description of expected value calculations followed by a section describing SEE ADC output comparisons and evaluation.

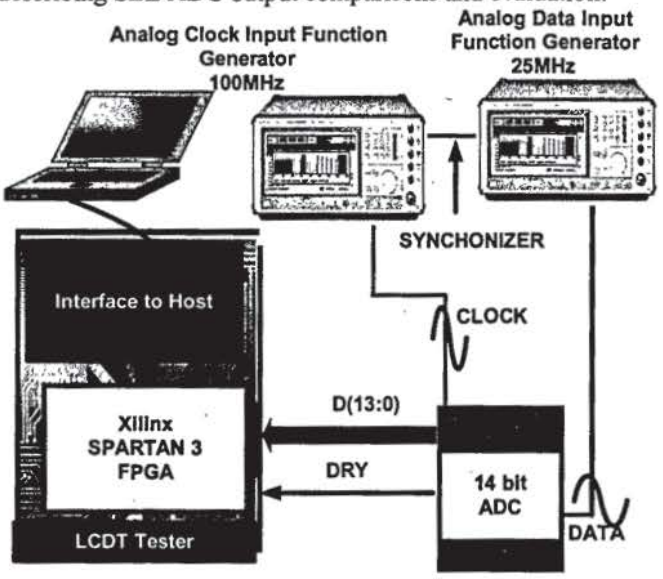

Fig. 5: LCDT Interface to DUT Schematic.

B. Expected Value Calculations

A window is defined to cover one complete period of the input signal and is illustrated in Fig. 6. Because there are 4 sample points per window regarding the FP scheme, one window will have 4 bins (k=0,1,2,3) – one for each input sample. Each Sample is accumulated into its designated bin (e.g. sample x_1 gets accumulated into bin k=1 and x_2 gets accumulated into bin k=2).

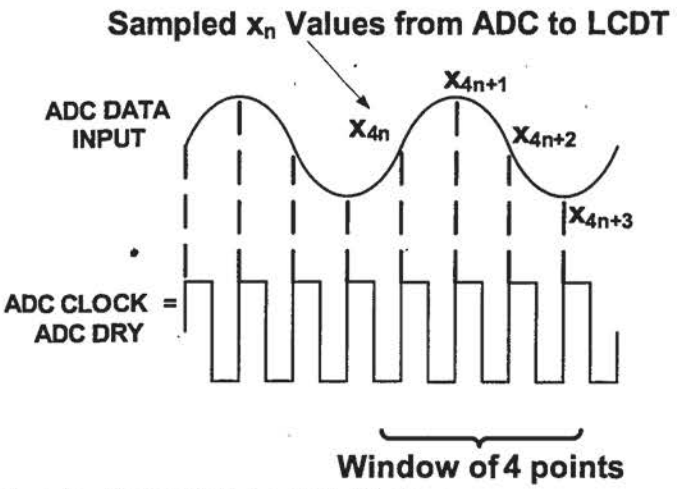

Fig. 6: Four Point ADC Clock and Data Waveforms.

The average of each bin produces 4 expected values with E = (E_0, E_1, E_2, E_3) and is reflected in (7).

$$E_k = \frac{\sum_{n=0}^{Total-1} x_{4n+k}}{Total}; \quad k = (0,1,2,3) \tag{7}$$

The tester calculates the four expected points by capturing 4.0×10^6 ADC output values. Hence, the total number of points for each of the 4 average calculations is 1.0×10^6. As previously stated, with proper system synchronization, the windowed ADC output codes will only deviate from the four calculated means by very small values. Therefore the usage of EB as with the SP and DP testing methods is also appropriate for FP. Expected values have been validated by observing that the ADC outputs always fall within small deviations from its reference after hours of operation. The EB is set to be greater than maximum deviation from mean. For the FP test vehicle, the minimal EB was calculated to be a code of 64 (4mv).

C. Data Compares to Expected Values during Irradiation

The ADC output code (x_n) is captured by the LCDT every ADC clock cycle. After capture, it is compared to its pre-calculated expected value to determine if there is a fault in the DUT output. The comparison is performed as follows: For each window of four points, compare incoming sample points ($x_{m \bmod k}$) to expected values (E_k) (e.g. compare x_1 to E_1). The comparison formula performed by the LCDT is found in (8). If the output value deviated greater than EB from its expected value, it was noted as an error.

$$(E_k - EB) < x_{m \bmod k} < (E_k + EB); \quad k = (0,1,2,3);\ m = (0,\infty) \tag{8}$$

D. Clock loss and Windowing

Because the analog data input is a sinusoid, without SEE, there is a strict ordering of ADC outputs within each 4-point window. The windowed ordering is based on point-to-point derivatives. Possible derivative orderings are listed in Fig. 7.

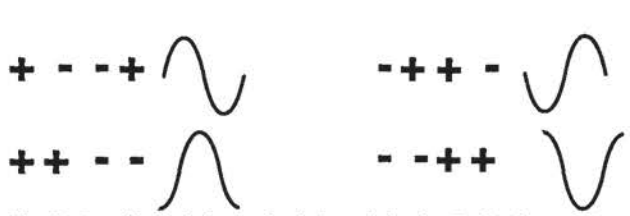

Fig. 7: Possible orderings of windowed 4-point Derivatives without error during Normal Operation.

Regarding Fig. 7, the sign of the derivative is of importance not the actual value. The sign can be obtained by subtracting x_{n-1} from x_n. If the ordering of the four windowed ADC output points is disrupted, then this can be an effect of clock loss or signal decomposition.

Clock loss can be detected by monitoring the DRY ADC output signal. As illustrated in Fig. 8, a clock loss can interrupt expected sequencing of incoming samples (to the tester). Once data sequencing has been interrupted, the tester comparison circuitry can not assume that the first value of the window will be associated with the original x_1 data item. If the tester is incapable of detecting and adjusting to this event, all comparisons thereafter will be incorrect and the test would have to be stopped. The LCDT handles such an event by first noting the upset. A dynamic synchronization scheme is then implemented to adjust to the new sequence ordering. The inclusion of dynamic synchronization elongates test time, increases SEE statistics, and provides a means to observe DUT recovery.

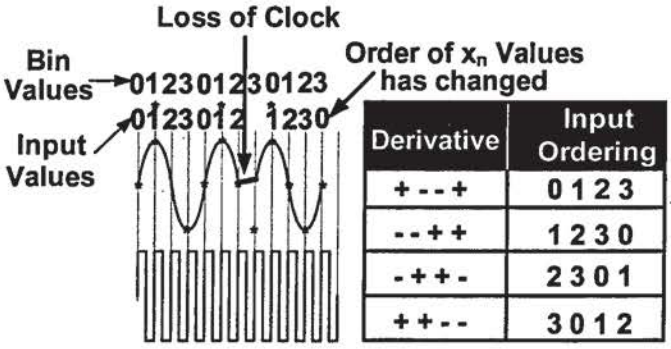

Fig. 8: FP Windows. Tester Synchronization Causes Order of Derivatives and Subsequent Expected Values to Change.

E. Clock Loss and Data Synchronization (Dynamic Windowing)

The previous section demonstrated how the order of ADC output values (tester input values) can change during a clock loss (e.g. E_1 no longer corresponds to x_1). In order to guarantee the correct sampled input is compared to the correct expected value, a novel approach had been developed called Dynamic Window Ordering (DWO). The 4 strict sequences (as illustrated in Fig. 7) of a sinusoidal input contained within each analysis window is the basis of DWO.

Each group of derivatives can directly be mapped into input

ordering schemes. The premise is illustrated in Fig. 8. The figure shows how the input sequence starts with x_1 with its associated derivative sequence (e.g. +--+ →0 1 2 3). This implies that as the input values are captured, they should be compared to expected values E_0, E_1, E_2, E_3. The derivative sequence is calculated for each window (i.e. for every 4 input values). If a clock loss occurs, the window derivative sequence will change depending on how many lost clock cycles had occurred and will be kept track of by the tester. The example in Fig. 8 shows one clock cycle loss that results in the following window having an input sequence of x_1, x_2, x_3, x_0 and after calculating the window derivatives, the inputs would thus be compared to the expected values: E_1, E_2, E_3, E_0.

V. Heavy Ion Test Results and Analysis

A. Test Facility and Test Parameters

Both of the DUTs (ADS5424 and ADC14155) were tested at the Texas A&M University Cyclotron Single Event Effects Test Facility using a 25MeV/u Tune at room temperature. All tests were run with 10^3<flux rate <10^4. LETs ranged from 2.5MeV*cm^2/mg to 60MeV*cm^2/mg.

B. Heavy Ion Results and Analysis for FP Test Data

Error signatures and their severity are important information that must be provided to design teams of critical systems. As previously stated, if a signal flattens or significant phase-shifts occur, the tests should be able to detect the events, their duration, and be able to differentiate such events. It will be demonstrated that the FP test methodology facilitates these requirements.

All graphs in this section that reflect ADC output codes versus time were constructed from FP SEU radiation tests. As described in the previous section, expected ADC output values were automatically calculated prior to each radiation test run by the LCDT. Graphs reflect erroneous ADC output codes accompanied by their expected code values. Each point on the graphs is an actual ADC output gathered by the LCDT. Prior to a SEE, the outputs are indistinguishable from their expected values as demonstrated in each graph. During error, the graphs illustrate the sampled outputs' deviation from expected values followed by their return to expected values. It should be noted that although the points are exact ADC output values, they are connected by an EXCEL fitting algorithm.

1) The Advantage of FP

Fig. 9 is a graph of flattening where the ADC eventually recovered with no intervention during the radiation test after 2.036us. It is noted that the DP method would not have detected the flattening. An error would have been generated at the start of the flattening because the x_n-x_{n-1} difference bound could not be satisfied. However, the following flattened data satisfies the difference therefore the severity of the error is not detected.

The signal is stretched in Fig. 10 and the signal is phase-shifted in Fig. 11. The SP and DP method would not be able to differentiate between a signal stretching and a signal flattening due to the under-sampling and lack of signal information.

After processing the error data from the FP SEE tests, the types of error signatures became apparent. Various error analyses followed such as the duration of the error (referred to as burst), analysis of signal distortion errors versus non-distorted errors, clock loss (ADC DRY signal), and phase analysis. The following section contains a couple of examples of how the FP SEE data has been further studied.

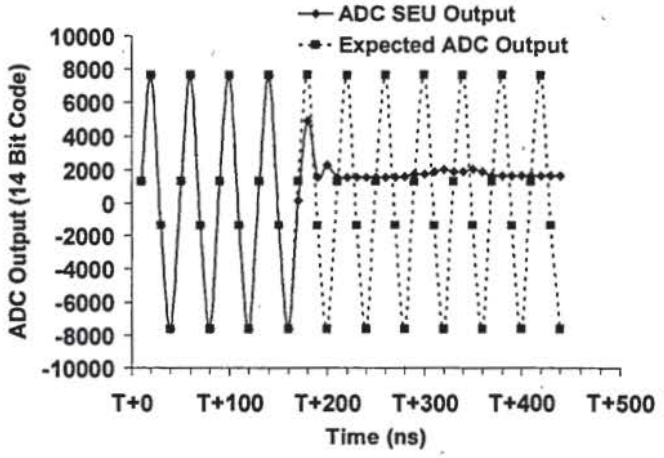

Fig. 9: SEU producing distorted ADC output at T+170ns. Signal eventually recovered to its expected value during the test after 2.036us. Internal ADC SEFI is most likely due to digital clock upset or PLL fault. LET=41.2MeV*cm^2/mg.

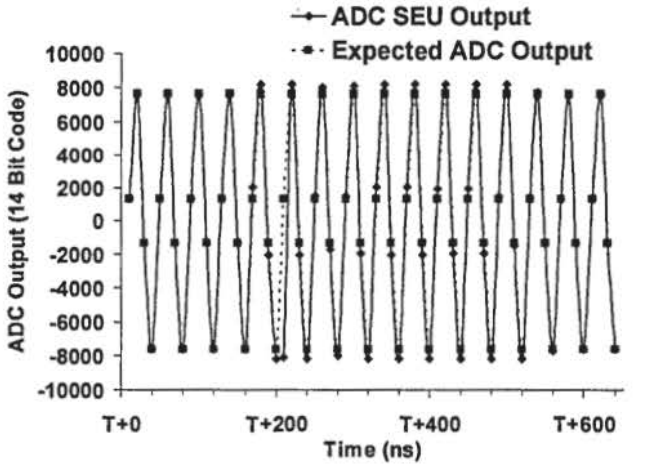

Fig. 10: SEU causing amplitude stretch with no phase shift in the TI ADS5424. Burst starts at T+170ns and is recovered to near its expected value at T+530ns. Most of the SEU amplitude code variations from expected values in this burst range from 550 to 750. LET=41.2MeV*cm^2/mg.

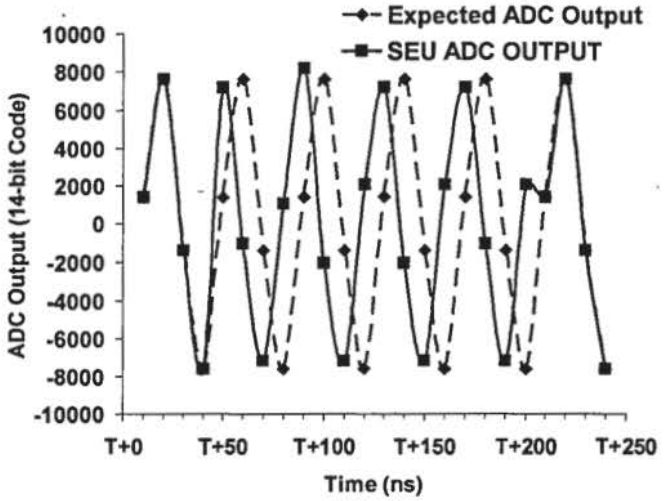

Fig. 11: SEU causing temporary phase shift in the TI ADS5424. Burst starts at T+50ns and is recovered to near its expected value at T+210ns. ADC Sample Clock Circuitry was affected. LET=41.2MeV*cm^2/mg.

2) The Advantage of FP

A burst is a string of consecutive ADC output code errors caused by one SEE. Many critical systems employ averaging or spectral analysis of ADC outputs over specified time periods. Erroneous ADC outputs that are infrequent or last for a relatively short period of time can generally be filtered. However, frequent or long bursts can be problematic. Hence, in order to not disrupt the digital processing of ADC outputs, understanding SEU burst lengths and their frequencies is essential. Fig. 12 and Fig. 13 are histograms demonstrating SEU burst Length for two separate LET values. In the histogram graphs, error event frequency has been normalized by particles per area and is hence an error cross-section. Bin 1 represents single cycle errors and therefore does not truly represent bursts. However, it is included as a comparison point. As expected, the frequency of all bursts are much lower for an LET of 2.5 MeV*cm^2/mg (Fig. 12) than 41.2 MeV*cm^2/mg (Fig. 13). It is interesting that at the lower LET the frequency of bursts that are less than or equal to 100 ADC clock cycles is greater than single cycle upsets. This phenomenon is most likely because the majority of the single-cycle faults are due to the digital portion of the ADC where as a significant portion of the bursts is due to the analog circuitry. This leads to the conclusion that the sensitivity of the analog circuitry at the lower LET is more significant than that of the digital.

The bin marked as "more" represents bursts that contained clock losses (no ADC DRY output) or bursts with very small error jittering around expected values. Upon clock loss, some events were able to recover within 100's of ADC input clock cycles (each clock cycle being 10ns). However, there were some clock losses that took micro-seconds to recover.

Most of the burst errors during irradiation for both DUTs (ADS5424 and ADC14155) were observed to be small perturbations to the internal ADC clock circuitry such that the output signal preserved its shape and amplitude yet its phase jittered around the expected value.

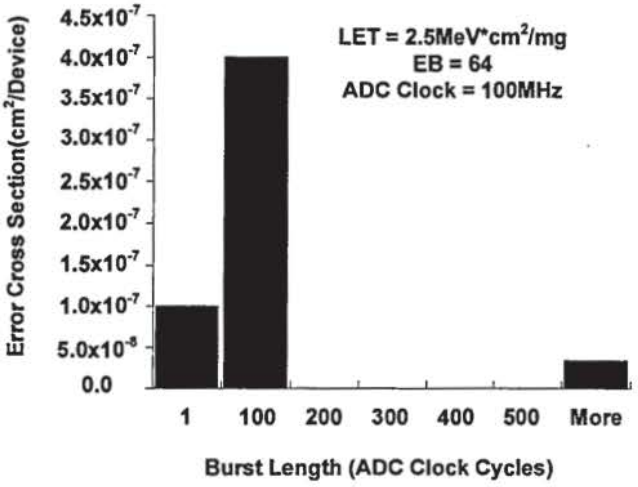

Fig. 12: Histogram of binned SEU burst lengths for LET=2.5MeVcm^2/mg. Event frequencies are normalized by radiation particles per area and are hence error cross-sections.

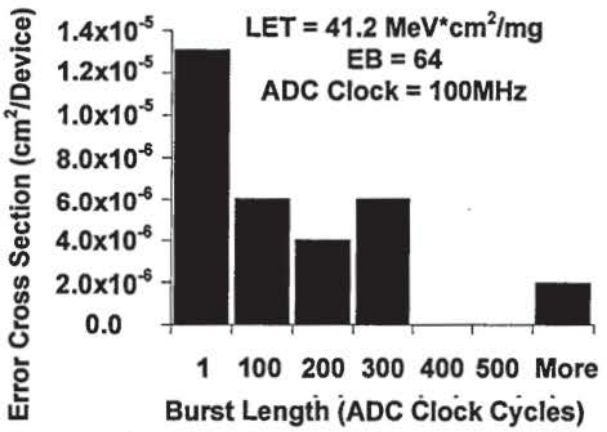

Fig. 13: Histogram of binned SEU burst lengths for LET=41.2MeVcm^2/mg. Event frequencies are normalized by radiation particles per area and are hence error cross-sections.

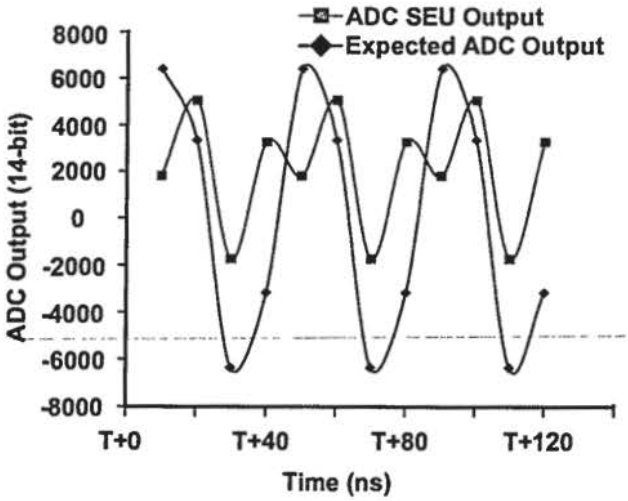

Fig. 14: Example of loss of signal composition in the ADC14155 due to a SEE during FP testing. Clock Sample rate was 100MHz and input sinusoid frequency was 25MHz. LET=41.5MeVcm^2/mg.

Distortion for this manuscript is defined as the ADC output

losing its shape, upon a SEU, and is thus a part of the signal composition evaluation process. The following are ADC outputs during SEE heavy-ion testing and provide clarity to the signal distortion definition. As previously discussed, Fig. 9 illustrates a distorted signal where flattening occurred during DUT irradiation. Fig. 14 is another example of signal distortion during SEE testing. Alternatively, Fig. 10 and Fig. 11 are examples of non-distorted SEEs. Fig. 10 demonstrates the ADC output being stretched following a SEU. For this example, the signal is considered not to be distorted. Fig. 11is an example of a phase-shifted signal, however, the signal has kept is composition and does not qualify as a distortion event. Each SEE test was analyzed to search for distorted versus non-distorted signal composition. Fig. 15 illustrates the SEU cross-sections of Distorted vs. Non-Distorted events. It is interesting that distortion clearly saturates at at-least 20 MeV*cm^2/mg. Below 20MeV*cm^2/mg, a significant number of distortions is evident and suggests that such events should be considered during the design process. Alternative cross-section comparisons and analyses can be conducted depending on the defined error conditions. One example would be to compare the cross-sections of phase shifted (non-distorted) signals versus all other burst error types.

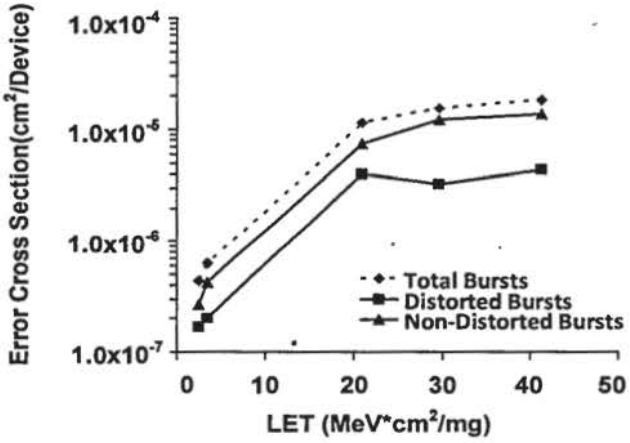

Fig. 15: Comparison of distorted versus non-distorted burst SEU cross-sections.

VI. Conclusion

Although informative, previous SEE ADC testing was unable to fully determine signal integrity such as phase shifts and signal composition due to the limited nature of static testing [1][2][3]. Other groups have started to implement conventional ADC manufacturer parametric algorithms (such as Beat Frequency [4] and DP) for SEE evaluation. Such tests have proven to be comprehensive for parametric measurements, but have also proven to have limitations with SEE characterization.

As previously stated, a myriad of test methodologies have been applied by various organizations. Due to the diverse nature of test vehicle implementation and input parameterization, SEE results become incomparable.

In response, REAG has begun development of ADC test methodology standardization. One of the techniques of the standardization package referred to as FP has been presented due to its robust effectiveness at fault observation. Heavy-Ion data obtained while implementing the FP technique was provided from testing ADC devices from two different manufacturers, Texas Instruments-ADS5424 and National Semiconductor-ADC14155. The results validated that the FP approach facilitates the observation of two-dimensional error signatures and signal composition during dynamic ADC testing and is therefore a significant enhancement to SEE data evaluation.

Although FP has proven to be an effective approach to signal composition analysis, it is not expected to be the sole SEE test of ADC circuitry. Instead, it is currently considered to be part of a package of tests required to comprehensively characterize SEE ADC response.

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